REMARKS

I. Status Summary

Claims 1-23 are pending in the instant application. Claims 1, 4-6, 8-11, 20, and 21 are amended herein. Claim 3 is canceled herein. Therefore, upon entry of this Amendment, Claims 1, 2, and 4-23 will be pending under consideration. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth herein below is respectfully requested.

II. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1-16 and 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art (hereinafter, "AAPA") in view of U.S. Patent No. 6,480,929 to Gauthier et al. (hereinafter, "Gauthier"). Claims 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Gauthier and further in view of U.S. Patent No. 5,400,369 to Ikemura (hereinafter, "Ikemura"). These rejections are respectfully traversed.

II.A. The Rejection Under 35 U.S.C. § 103 as Being Unpatentable Over Dudley In View of Anderson

Regarding Claim 1, the Examiner contends that AAPA teaches all of the features recited in Claim 1 except "the data memory having its own 'data memory address bus in a data address space' to the data processing unit". Official Action, pages 2 and 3. In

addition, the Examiner contends that AAPA also fails to disclose "the input and output interface buffers having their own 'interface address bus in an independent interface address space' connected to the data processing unit". Official Action, page 3. The Examiner also contends that Gauthier teaches the use of two independent, separate and distinct address busses by a processor to communicate with two modules. Official Action, page 3. Further, the Examiner contends that the use of the two different busses allow for address communication to happen concurrently for allowing one of the module to get data ready for transmission without much lag after the other module has completed data transmission. Official Action, page 3. The Examiner contends that it would have been obvious to one of ordinary skill in the art to combine the teachings of both AAPA and Gauthier to provide two separate independent busses, a "data memory address bus in a data address space", and an "interface address bus in an independent interface address space" because it would allow for concurrent communication on the address busses, thus allowing for reduction in latency and wait states. Official Action, page 3.

II.B. Applicants' Response

Claims 2-16 and 20-23 depend from Claim 1. Claim 1 has been amended to recite a high speed process having (1) at least one input buffer which is connected to a data bus and has the purpose of buffering input data; (2) at least one output interface buffer which is connected to the data bus and has the purpose of buffering output data;

(3) a ROM memory for storing program data which is connected to the data processing unit via lines; and (4) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via a separate interface address bus in an independent interface address space. Summarily, neither AAPA nor Gauthier, alone or in combination, discloses all of the features recited in Claim 1. Additionally, neither AAPA nor Gauthier offers suggestion to modify the devices or methods disclosed therein to arrive at the presently claimed subject matter.

Regarding AAPA, the Examiner refers to Figure 2 of the present application. AAPA discloses a single address bus **39** for addressing data memory **41** and ports **38** and **40**. Present Application, page 2, lines 2-29, and Figure 2. Additionally, the Examiner notes that data memory **41** and input and output ports **38** and **40** all connect to address bus **39**. Official Action, page 3. AAPA does not disclose that input interface buffer **9** and output interface buffer **26** of process **1** are directly addressable by data processing unit **13** via a separate interface address bus **24** in independent interface address space. On the other hand, Claim 1 in element (f) has been amended to recite that the input interface buffer and the output interface buffer is directly addressable by the data processing unit via a separate interface address bus in an independent interface address space. The subject matter of element (f) is advantageous, for example, because it provides for high speed processing which permits data transfer at a very high transmission rate. Applicants respectfully submit that the features recited in element (f) of Claim 1 are not disclosed or suggested by AAPA. Additionally, AAPA

offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention.

Gauthier fails to overcome the significant shortcomings of AAPA. Gauthier is directed to a microcontroller **M** connected to a dynamic random access memory **200** or other volatile memory, and a read only memory (ROM) **202** or other volatile memory. Gauthier, column 4, lines 61-66, and Figure 2A. Microcontroller **M** controls access to DRAM **200** and ROM **202**. Gauthier, column 4, lines 66 and 67. DRAM **200** and ROM **202** share a data bus DATA coupled to microcontroller **M**. Gauthier, column 4, line 67, to column 5, line 2. Microcontroller **M** is coupled to the data bus DATA through signal pins **204** shared by DRAM **200** and ROM **202**. Gauthier, column 5, lines 2-4. A DRAM address bus (DRAM_ADD) and a DRAM control bus (DRAM_CTL) are provided between microcontroller **M** and DRAM **200**. Gauthier, column 5, lines 14-19. In addition, a ROM address bus (ROM_ADD) and a ROM control bus (ROM_CTL) connect microcontroller **M** and ROM **202**. Gauthier, column 5, lines 19-22. Applicants submit that Gauthier does not disclose or suggest input and output interface buffers which are connected to a data bus and have the purpose of buffering input and output data, respectively, as recited by elements (c) and (d) of Claim 1.

In addition, applicants respectfully submit that Gauthier does not disclose or suggest the features recited in element (f) of Claim 1. Element (f) of Claim 1 recites that the input interface buffer and the output interface buffer is directly addressable by the data processing unit via a separate interface address bus in an independent interface

address space. The input and output interface buffers are recited in elements (c) and (d). Therefore, because Gauthier does not disclose or suggest the input and output interface buffers recited in elements (c) and (d) of Claim 1, Gauthier cannot disclose or suggest the features recited in element (f) of Claim 1. Accordingly, Claim 1 is believed to be patentably distinguished over the combination of AAPA and Gauthier. Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claims 2-16 and 20-23 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 2-16 and 20-23. Thus, Claims 2-16 and 20-23 are believed to be patentably distinguished over AAPA and Gauthier. Applicants respectfully request that the rejection of Claims 2-16 and 20-23 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

II.C. The Rejection Under 35 U.S.C. § 103 as Being Unpatentable Over Dudley In View of Gauthier and Further In View of Ikemura

Regarding Claims 17-19, the Examiner contends that AAPA discloses the high speed processor having a data frame detecting device but does not explicitly disclose the details about the frame detecting device as recited in Claim 16. Official Action, page 5. The Examiner contends that Ikemura discloses the details of the frame detecting device as recited in Claims 17 and 18 and that it would have been obvious to one of ordinary skill in the art to apply the teachings of Ikemura to the combination of AAPA

and Gauthier to achieve the subject matter recited in Claims 17 and 18. Official Action, page 6. Regarding Claim 19, the Examiner contends that it is well known in the art to output modulated data such as PCM data through a medium and that it would have been obvious to one of skill in the art to implement the output interface buffer as a PCM interface buffer for buffering PCM data. Official Action, page 6.

II.D. Applicants' Response

Claims 17-19 depend from Claim 1. As noted above, Claim 1 has been amended to recite a high speed process having (1) at least one input buffer which is connected to a data bus and has the purpose of buffering input data; (2) at least one output interface buffer which is connected to the data bus and has the purpose of buffering output data; (3) a ROM memory for storing program data which is connected to the data processing unit via lines; and (4) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via a separate interface address bus in an independent interface address space. Summarily, neither AAPA, Gauthier, nor Ikemura, alone or in combination, discloses all of the features recited in Claim 1. Additionally, neither AAPA, Gauthier, nor Ikemura, offers suggestion to modify the devices or methods disclosed therein to arrive at the presently claimed subject matter.

Ikemura fails to overcome the significant shortcomings of AAPA and Gauthier described above. Ikemura is directed to a frame detecting device that can recognize data formats. The frame detecting device includes a shift register **101** that receives

byte-wide input data. Ikemura, column 2, lines 64 and 65, and Figure 2. The first fifteen bits of byte register **101** are provided in parallel form as test data B to a data scanner **102** and as intermediate data C to an aligner **104**. Ikemura, column 3, lines 2-5. Data scanner **102** searches for the value A1 in the test data B received from shift register **101** by comparing A1 with bits 1-8, with bits 2-9, etc. Ikemura, column 3, lines 6-10. Data scanner **102** can perform these eight comparisons simultaneously and output the result as alignment data D and E. Ikemura, column 3, lines 10-13. Applicants submit that Ikemura does not disclose or suggest input and output interface buffers which are connected to a data bus and have the purpose of buffering input and output data, respectively, as recited by elements (c) and (d) of Claim 1. In addition, Ikemura does not disclose or suggest the additional features of the input and output interface buffers as recited in element (f) of Claim 1.

Claims 17-19 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 17-19. Thus, Claims 17-19 are believed to be patentably distinguished over AAPA, Gauthier, and Ikemura. Applicants respectfully request that the rejection of Claims 17-19 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

III. Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

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DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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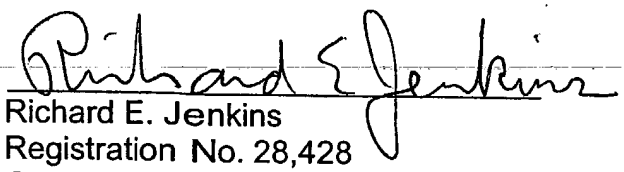
Date: July 14, 2004 By: 

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